REMARKS

Claims 1-4 are all the claims pending in the application.

The Examiner rejects claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Blinne et al. (U.S. Patent 5,274,568) in view of Hasegawa '168 (U.S. Patent 6,041,168) and further in view of Hasegawa '511 (U.S. Patent 5,528,511).

Applicant respectfully traverses this rejection. The combination of Blinne, Hasegawa '168, and Hasegawa '511 does not teach or suggest all of the claimed features of Applicant's invention. Claims 1-4 are independent claims, and claims 2-4 recite a system, method and medium, respectively, that share many of the same features of claim 1. Therefore, Applicant arguments in traverse of the rejection will focus on claim 1.

The Examiner acknowledges that Blinne does not disclose or suggest the feature of claim 1 of "said library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal" (see also claims 2-4). The Examiner alleges that Hasegawa '168 discloses this feature. Applicant respectfully disagrees.

Hasegawa '168 does not disclose that logical operation information is stored in a delay analysis library as required by the claim. In fact, Hasegawa '168 does not disclose a delay analysis library at all. Furthermore, Hasegawa '168 does not disclose logical operation information "representing a correspondence between a logical value of each input terminal and the logical value of the output terminal" as required by claim 1. Hasegawa '168 discloses storing

a delay model that simply models the physical structure of the logic circuit (Hasegawa '168, column 4, line 57 through column 5, line 12), not its logical operation.

Figure 3 shows an example of this delay model in which the nodes 301-311 correspond to the pins 21-25 of the logic circuit. But the logical values of the terminals are not stored in Hasegawa '168. In fact, the logical values of the terminals are not used in the delay time calculation at all (See Hasegawa '168, column 5, line 41 through column 7, line 53).

Therefore, Hasegawa '168 does not supply at least this deficiency in Blinne with respect to claim 1. Claims 2-4 include features similar to this feature of claim 1 discussed above. Therefore, claims 2-4 are allowable at least for the reasons discussed above with respect to claim 1.

Furthermore, one of skill in the art would not have been motivated to combine the references as the Examiner suggests. For example, even if, assuming *arguendo*, Hasegawa '168 did disclose logical operation information, nothing in either Blinne or Hasegawa would suggest that that logical operation information be stored in the cell library of Blinne. In fact, because each of Blinne, Hasegawa '168, and Hasegawa '511 disclose a fully functional system for determining the delay time of a logic circuit that is incompatible with the others, there would be no motivation to combine the references at all. For example, Blinne estimates the delay time based on the delay time of the rising edge or the falling edge of a signal through part of a circuit (Blinne, column 1, lines 37-52). Hasegawa '168, however, relates to verifying the delay time of a circuit by obtaining the maximum delay time of a node in a physical model of a circuit, and approving or disapproving of nodes in that model whose maximum delay time exceeds a

predetermined limit (Hasegawa '168, column 4, lines 4-12). Hasegawa '511, by contrast, verifies the delay time of a circuit by modeling the circuit using graph theory, resulting in a graph theoretical circuit model different from the physical circuit model of Hasegawa '168 (Hasegawa '511, column 1, lines 8-13).

Each reference discloses a functioning delay time analysis system, so there would be no motivation to combine parts of the system of one reference with the complete and functioning system of another. None of the references contain any suggestion that would motivate such a combination, and it is likely that combining the parts of the system of one reference with those of another could render an otherwise functioning delay analysis system inoperable.

Because it would not have been obvious to one of skill in the art at the time of the invention to combine the references, the rejection of claims 1-4 under 35 U.S.C. § 103(a) is traversed at least for this reason. Applicant therefore submits that claims 1-4 should be allowed.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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